On homogeneous matroid ports*

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Abstract

A matroid port is a clutter (antichain of sets) determined by the collection of circuits of a matroid that contain a fixed point. We study the problem of determining matroid ports all whose elements have the same size h. This problem has been studied from the cryptographic perspective and it is related to an analogous problem in matroid theory. We give some general results and then focus on the binary case. We recast some known results and find all 4-homogeneous binary matroid ports.

1 Introduction

A *clutter* is a collection of sets that are mutually incomparable with respect to inclusion; the *support* of a clutter Δ is $\cup_{A\in\Delta}A$. For a matroid $\mathcal{M}$ on the ground set E, the collection of its circuits $\mathcal{C}(\mathcal{M})$ forms a clutter (as do the collections of bases or hyperplanes). We are interested in another clutter derived from the circuits of a matroid. For an element $p \in E$, the *matroid port of* $\mathcal{M}$ *at* p is the clutter $\mathcal{M}_p$ defined as[1]

$$\mathcal{M}_p = \{C - p : C \in \mathcal{C}(\mathcal{M}), p \in C\}.$$

A clutter Δ with support Ω is said to be a *matroid port* if Δ is the port of some matroid $\mathcal{M}_\Delta$ with ground set $E = \Omega \cup p$ with $p \notin \Omega$ (we refer to Section 2 for more details on how $\mathcal{M}_\Delta$ is constructed). Matroid ports were introduced by Lehman [2] in connection with game theory, and they are a key structure in the theory of secret sharing [6], both for the characterization of ideal access structures and to obtain bounds on the optimal information rate of the scheme.

In this paper we focus on the problem of determining the matroid ports all whose elements have the same size. We say that a clutter Δ is h-homogeneous if $|A| = h$ for all $A \in \Delta$, and we call h the *rank* of the clutter[2]. Our motivation for studying this problem is twofold, as we next explain.

A particular family of h-homogeneous matroid ports are those that arise as ports of matroids all whose circuits have size $h + 1$. Unfortunately, determining such matroids is a hard problem. In [8], Murty determined the binary matroids all whose circuits have a given size. As we will see throughout this work, there are usually many more h-homogeneous binary matroid ports than matroids all whose circuits have size $h+1$, since being an h-homogeneous matroid port only gives information on the sizes of the circuits that contain p. In particular, for even h it is proved in [8] that there is only one binary matroid with circuits of size $h + 1$ (a single circuit), but we will see in Section 4 that 4-homogeneous

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[1]We use the common convention in matroid theory to write $A - b, A \cup b$ instead of $A - \{b\}, A \cup \{b\}$.

[2]In the few places we use the word "rank" to refer to the rank of a matroid it will be said clearly.

binary matroid ports are much richer. The question of determining matroids whose circuit-sizes belong to a small, fixed set, has also been studied [3], but the results do not seem applicable in our situation.

In addition to the relationship with the purely matroid theoretic question studied by Murty, the problem of determining h-homogeneous matroid ports is of interest in the context of secret sharing schemes in cryptography. Specifically, from the results in [6] it follows that to provide a complete description of h-homogeneous matroid ports is equivalent to characterizing the access structures of the ideal secret sharing schemes whose minimal qualified subsets have h participants. As far as we know, the only results in this direction have been obtained in [1, 4, 5] for the cases $h = 2$ and $h = 3$. The tools used in these works are mostly of a cryptographic nature. It is also one of our goals to present these results in a unified, more combinatorial way.

This work has two main contributions. First, we develop some reductions and general results that are applicable to any h and to all kind of ports, whether binary or not. Then, we treat the concrete case of $h = 4$ in the binary case, providing a complete description of 4-homogeneous binary matroid ports. The proofs will be included in a full version of this extended abstract.

We conclude this introduction by mentioning that we are not aware of results for the case $h \geqslant 5$ in general, or for the non-binary case for $h = 3, 4$. We feel that many of our techniques can be applied in the binary case for $h \geqslant 5$, but we are far from even conjecturing a list of 5-homogeneous binary matroid ports.

2 Preliminaries and reductions

We review in this section several results and characterizations about matroid ports and binary matroid ports. We refer to Oxley's book [9] for all terms and results in matroid theory.

A connected matroid $\mathcal{M}$ is determined by any one of its ports $\mathcal{M}_p$. We state next the description of the circuits of $\mathcal{M}$ in terms of the sets in the port. We use the notation $A_1 \ominus A_2$ to denote the symmetric difference of A_1 and A_2. Also, by $\min(\{B_1, \ldots, B_m\})$ we denote the inclusion minimal elements of $\{B_1, \ldots, B_m\}$.

Theorem 1. *([2], [9, Thm. 4.3.3]) Let Δ be a matroid port with support Ω. Then there is a unique connected matroid $\mathcal{M}_\Delta$ on $\Omega \cup p$. Moreover, the circuits of $\mathcal{M}_\Delta$ are*

$$\mathcal{C}(\mathcal{M}_\Delta) = \big\{A \cup p \,:\, A \in \Delta\big\} \cup \min(\big\{A_1 \ominus_\Delta A_2 \,:\, A_1, A_2 \in \Delta, A_1 \neq A_2\big\}),$$

where

$$A_1 \ominus_\Delta A_2 = (A_1 \cup A_2) \setminus \bigcap_{\substack{A \subseteq A_1 \cup A_2 \\ A \in \Delta}} A.$$

A clutter Δ on a finite set E is said to be a $\mathbb{K}$-*representable matroid port* if it is the port of a matroid $\mathcal{M}$ representable over the field $\mathbb{K}$. In particular, $\mathbb{F}_2$-representable matroid ports will be called *binary*.

Before stating characterizations for matroid ports and binary matroid ports, we need one more definition. The *blocker* of a clutter Δ on E is the clutter $b(\Delta) = \min\left(\{B \subseteq E : B \cap A \neq \emptyset \text{ for all } A \in \Delta\}\right)$. It is well-known that $b(b(\Delta)) = \Delta$. For matroid ports, it is not difficult to check that $b(\mathcal{M}_p) = (\mathcal{M}^*)_p$, where $\mathcal{M}^*$ is the dual of $\mathcal{M}$. Thus, the blocker of a matroid port is again a matroid port. As the dual of a $\mathbb{K}$-representable matroid is also $\mathbb{K}$-representable, the blocker of a binary matroid port is also a binary matroid port. Note though that the blocker of an h-homogeneous clutter need not be homogeneous.

Theorem 2. *1. The clutter Δ is a matroid port if and only if whenever $A_1, A_2, A_3 \in \Delta$ and $x \in (A_2 \cap A_3) \setminus A_1$ there is $A \in \Delta$ with $A \subseteq \big((A_1 \ominus_\Delta A_2) \cup A_3\big) \setminus \{x\}$.*

2. The clutter Δ is a binary matroid port if and only if either of the following two statements holds:

(a) For all $A \in \Delta$ and for $B \in b(\Delta)$ the intersection $A \cap B$ has odd cardinality.

(b) If $A_1, A_2, A_3 \in \Delta$, then there exists $A \in \Delta$ with $A \subseteq A_1 \ominus A_2 \ominus A_3$.

For a proof of this theorem, we refer to [10] and [11]. We mention that there are several other characterizations of matroid ports that range from excluded minors [10, 11] to independent sequences and bounds on the optimal information rates in secret sharing schemes [6, Theorem 4.4]. Although we do not use these characterizations, we use the notion of minors of matroid ports in some constructions, so we review them here.

Let Δ be a clutter with support Ω and let $Z \subset \Omega$. The *deletion of* Z is the clutter $\Delta \setminus Z$ given by $\Delta \setminus Z = \{A \subseteq \Omega \setminus Z : A \in \Delta\}$; we refer to the clutter $\Delta \setminus (\Omega \setminus Z)$ as the *restriction* of Δ to Z, denoted by $\Delta|Z$. The *contraction of* Z is the clutter Δ/Z given by $\Delta/Z = \min(\{A \subseteq \Omega \setminus Z : A \setminus Z \in \Delta\})$. When Δ is the clutter of circuits of a matroid, these definitions give the usual notions of deletion and contraction in matroids (and we write $\mathcal{M}/Z$ instead of $\mathcal{C}(\mathcal{M})/Z$, and so on). Every clutter that can be obtained from Δ by repeatedly applying the operations $\setminus$ and $/$ is called a *minor* of Δ. Minors of matroid ports are matroid ports: indeed, we have $\mathcal{M}_p \setminus Z = (\mathcal{M} \setminus Z)_p$ and $\mathcal{M}_p/Z = (\mathcal{M}/Z)_p$.

We say that the clutter Δ is *path-connected* if for all $x, y \in \Omega$ there is a sequence $A_1, \ldots, A_k$ with $A_i \in \Delta$, $x \in A_1$, $y \in A_k$ and $A_i \cap A_j \neq \emptyset$ (if the sets of the clutter are thought of as the hyperedges of a hypergraph, path-connectivity becomes connectivity in the hypergraph). We say that x and y are at distance k in Δ if k is the smallest integer for which such a sequence exists. For any clutter Δ there exists a unique partition $\Omega = \Omega_1 \cup \cdots \cup \Omega_s$ such that the restrictions $\Delta|\Omega_1, \ldots, \Delta|\Omega_s$ are path-connected and $\Delta = \Delta|\Omega_1 \cup \cdots \cup \Delta|\Omega_s$. In this situation we say that $\Delta|\Omega_1, \ldots, \Delta|\Omega_s$ are the *path-connected components* of Δ. It is clear that a clutter is h-homogeneous if and only if each of its path-connected components is h-homogeneous.

In the particular case that the clutter is a matroid port $\mathcal{M}_p$, being path-connected is equivalent to the matroid $\mathcal{M}$ not being a parallel connection of two smaller matroids (see [9, Sec. 7.1] for the definition and properties of parallel connection). From this one obtains the following characterization.

Lemma 3. *Let Δ be a clutter whose path-connected components are $\Delta_1, \ldots, \Delta_m$. Then Δ is a matroid port if and only if $\Delta_1, \ldots, \Delta_m$ are matroid ports. Moreover, for any field $\mathbb{K}$, Δ is a $\mathbb{K}$-representable matroid port if and only if $\Delta_1, \ldots, \Delta_m$ are $\mathbb{K}$-representable matroid ports.*

It was shown in [7] that the diameter of a path-connected matroid port is at most two (by the diameter we mean, as usual, the maximum of the distances). The following lemma gives a condition for adding sets to an h-homogeneous binary matroid port of diameter 2 so that the result is an h-homogeneous binary matroid port of diameter 1. The proof is based on checking condition 2.(a) in Theorem 2.

Lemma 4. *Let Δ be a path-connected, h-homogeneous binary matroid port with support Ω such that its blocker $b(\Delta)$ contains the pairs $\{x_1, y_1\}, \{x_2, y_2\}, \ldots, \{x_s, y_s\}$ (with all the x_i, y_i different among them). Then $s \leqslant h$. For $s = h$, let $z_3, \ldots, z_h \notin \Omega$ and define $\Delta' = \Delta \cup \{\{x_i, y_i, z_3, \ldots, z_h\} : 1 \leqslant i \leqslant h\}$. If $b(\Delta)$ contains no set of the form $\{v_1, \ldots, v_t\}$ with $v_i \in \{x_i, y_i\}$ and $t < h$ then the clutter Δ' is an h-homogeneous binary matroid port.*

In addition to restricting to path-connected clutters, we introduce some other reductions. Two elements x, y in a clutter Δ are *equivalent* if for any $A \in \Delta$ we have $|A \cap \{x, y\}| \leqslant 1$, and if $|A \cap \{x, y\}| = 1$ then $A \ominus \{x, y\} \in \Delta$. It is easy to check that equivalent elements in a matroid port $\mathcal{M}_p$ correspond to parallel elements in $\mathcal{M}$. An element q in a clutter is called *universal* if $q \in \bigcap_{A \in \Delta} A$. If a matroid port $\mathcal{M}_p$ has a universal element q, then $\{p, q\}$ are a series pair in $\mathcal{M}$ (a parallel pair in $\mathcal{M}^*$). The *reduction* of a clutter Δ is the clutter Δ^{red} obtained by removing all but one copy of each equivalence class and removing all universal elements.

Lemma 5. *A clutter Δ is a matroid port (resp. is a $\mathbb{K}$-representable matroid port) if and only if its reduced clutter Δ^{red} is so. Moreover, if Δ has exactly t universal elements, then Δ is h-homogeneous if and only if Δ^{red} is $(h - t)$-homogeneous.*

We say that a clutter is *reduced* if it is path-connected and $\Delta^{\text{red}} = \Delta$. By Lemmas 3 and 5, we can restrict to h-homogeneous reduced matroid ports (although in some of the results in the following section we drop this restriction if the result is sufficiently simple to state it in general).

3 Homogeneous matroid ports of ranks 1, 2, 3, $n-1$ and n

Let Δ be an h-homogeneous clutter with support Ω, where $|\Omega| = n$. For $h = 1$ and $h = n$, the characterizations of Theorem 2 imply that $\Delta = \big\{\{x_1\}, \ldots, \{x_n\}\big\}$ and $\Delta = \big\{\{x_1, \ldots, x_n\}\big\}$ are binary matroid ports. The following proposition deals with the case $h = n-1$. The proof consists in checking that the collection $\mathcal{C}(\mathcal{M}_\Delta)$ as in Theorem 1 is indeed the collection of circuits of a matroid.

Proposition 6. *Let Δ be an $(n-1)$-homogeneous clutter with support Ω with $n = |\Omega|$. Then, Δ is a matroid port. Furthermore, Δ is a binary matroid port if and only if $|\Delta| = 2$.*

Now let us consider the case $h = 2$. Note that a 2-homogeneous clutter with support Ω can be thought of as the edges of a graph with vertex set Ω (and no isolated vertices). For the complete multipartite graph $G = K_{n_1,\ldots,n_\ell}$, for $\ell \geqslant 2$ and $n_i \geqslant 1$, the clutter $E(G)$ is a matroid port. Indeed, the reduced clutter $E(K_{n_1,\ldots,n_\ell})^{\text{red}}$ is the set of edges of a complete graph K_ℓ, and $E(K_\ell)$ is the port of a uniform matroid $U_{2,\ell+1}$ at any of its points. By adding equivalent elements we obtain $E(K_{n_1,\ldots,n_\ell})$. As $U_{2,4}$ is the excluded minor for binary matroids, the only one of these ports that is binary is $E(K_{n_1,n_2})$.

The following result states that these are the only 2-homogeneous matroid ports. It can be proved directly by using the characterizations of matroid ports in the previous section, or by combining results about secret sharing schemes from [1] and [6].

Theorem 7. *Let Δ be a path connected 2-homogeneous clutter. Then Δ is a matroid port if and only if Δ is isomorphic to $E(K_{n_1,\ldots,n_\ell})$, and it is is a binary matroid port if and only if Δ is isomorphic to $E(K_{n_1,n_2})$.*

Finally, in Theorem 8 we present the description of 3-homogeneous reduced binary matroid ports. The clutters involved in this theorem are defined as follows. The clutter $\Delta_{3,0}$ is the clutter whose elements are the 7 lines of the Fano plane; that is, $\Delta_{3,0} = \{\{a_1, a_2, a_3\}, \{a_1, a_4, a_7\}, \{a_1, a_5, a_6\}, \{a_2, a_4, a_6\}, \{a_2, a_5, a_7\}, \{a_3, a_4, a_5\}, \{a_3, a_6, a_7\}\}$ (as noted in [5], $\Delta_{3,0}$ is the port of the binary affine cube $\mathrm{AG}(3,2)$ at any of its points). The clutter $\Delta_{3,1}$ is $\Delta_{3,0} \setminus a_7$ (which can also be thought of as the set of 3-cycles of K_4). We remark that $\Delta_{3,0}$ can be constructed from $\Delta_{3,1}$ by using Lemma 4 (and checking first that $\Delta_{3,1}$ is binary, for instance by using Theorem 2).

Theorem 8. *Let Δ be a reduced 3-homogeneous clutter. Then, Δ is a binary matroid port if and only if Δ is isomorphic either $\Delta_{3,0}$ or $\Delta_{3,1}$.*

There are several ways of proving this theorem; one of them is by carefully analysing the circuits of $\mathcal{M}_\Delta$ as given by Theorem 1 and showing that if Δ is a 3-homogeneous binary matroid port, then $\mathcal{M}_\Delta$ is a matroid all whose circuits are of size 4. Thus, one can then apply the results by Murty [8].

Alternatively, Theorem 8 follows from the results in [5] and [6] by relating matroid ports to ideal secret sharing schemes. Moreover, from these papers one can show that if Δ a 3-homogeneous non-binary matroid port then Δ is the port of a matroid of rank three. An example is the clutter defined by the non-Pappus configuration, obtained by taking all 3-element subsets of a set of size 9 except those that are lines in the non-Pappus matroid (see [5, Example 3.5]). As far as we know, the complete description of non-binary 3-homogeneous matroid ports is an open problem.

4 Homogeneous binary matroid ports of rank 4

For 4-homogeneous matroid ports, there are no known results from the secret sharing community, and the results from [8] do not shed much light, as there is only one binary matroid all whose circuits have

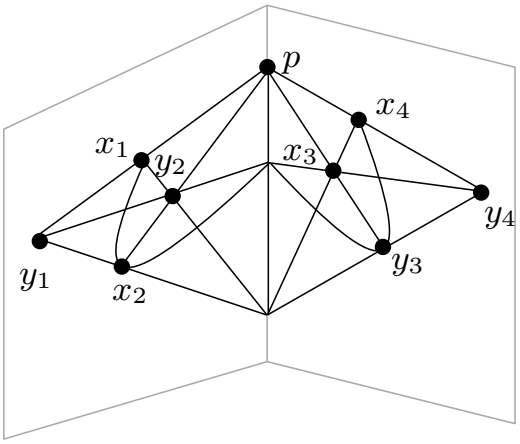

Figure 1: A geometric representation of the binary 4-spike. The hyperplanes avoiding p are in bijection with the sets in the port $\Delta_{4,1}$.

size 5 (namely, a single 5-circuit). Note that the corresponding matroid port has just one set, a case already commented at the beginning of Section 3.

Before stating our main result, we need to introduce yet one more reduction, which can be seen as an extension of equivalent elements.

Let Δ be a 4-homogeneous binary matroid port. We say that the pairs $\{a_1, a_2\}$ and $\{b_1, b_2\}$ are *clones* if the following three conditions hold

- $|A \cap \{a_1, a_2, b_1, b_2\}| \neq 1$ for all $A \in \Delta$;
- $\{a_i, b_j\} \not\subseteq A$ for any $A \in \Delta$ and $1 \leqslant i, j \leqslant 2$;
- $\{a_1, a_2, x, y\} \in \Delta$ if and only if $\{b_1, b_2, x, y\} \in \Delta$ for all $x, y \in E$.

Since the property of being binary and 4-homogeneous is preserved under deletion, the removal of one of the pairs $\{a_1, a_2\}$ or $\{b_1, b_2\}$ still leaves a binary 4-homogeneous matroid port. Next we consider the reverse process, that is, when it is possible to add a pair of clones. The proof of the following lemma consists in checking condition 2.(b) in Theorem 2.

Lemma 9. *Let Δ be a binary 4-homogeneous matroid port such that there are two elements $\{a_1, a_2\}$ with the property that $|A \cap \{a_1, a_2\}| \in \{0, 2\}$ for all $A \in \Delta$. Let b_1, b_2 be two elements not in the support of Δ. Then the clutter $\Delta' = \Delta \cup \{A \setminus \{a_1, a_2\} \cup \{b_1, b_2\} \mid \{a_1, a_2\} \subseteq A \in \Delta\}$ is binary.*

Thus, we can assume that Δ is clone-free. Theorem 10 states that there are only four 4-homogeneous binary matroid ports that are reduced and clone-free. We next define these four clutters, and show that they are indeed binary.

The clutter $\Delta_{4,1}$ is the following

$$\begin{aligned}\Delta_{4,1} = \{&\{x_1, x_2, y_3, x_4\}, \{x_1, x_3, y_2, x_4\}, \{x_2, x_3, y_1, x_4\}, \{y_1, y_2, y_3, x_4\},\\ &\{x_1, y_2, y_3, y_4\}, \{x_2, y_1, y_3, y_4\}, \{x_3, y_1, y_2, y_4\}, \{x_1, x_2, x_3, y_4\}\}.\end{aligned}$$

It is a binary matroid port since $b(\Delta_{4,1})$ is the port of the binary 4-spike at its tip (Figure 1 shows a geometric representation of the binary 4-spike; the elements of $\Delta_{4,1}$ are given by the complements of the planes that do not contain p, with p removed).

If we apply Lemma 4 to $\Delta_{4,1}$, we obtain the binary matroid port $\Delta_{4,0}$:

$$\begin{aligned}\Delta_{4,0} = \{&\{x_1, x_2, y_3, x_4\}, \{x_1, x_3, y_2, x_4\}, \{x_2, x_3, y_1, x_4\}, \{y_1, y_2, y_3, x_4\},\\ &\{x_1, y_2, y_3, y_4\}, \{x_2, y_1, y_3, y_4\}, \{x_3, y_1, y_2, y_4\}, \{x_1, x_2, x_3, y_4\},\\ &\{x_1, y_1, z_1, z_2\}, \{x_2, y_2, z_1, z_2\}, \{x_3, y_3, z_1, z_2\}, \{x_4, y_4, z_1, z_2\}\}.\end{aligned}$$

Finally, $\Delta_{4,2} = \Delta_{4,0} \setminus x_4$ and $\Delta_{4,3} = \Delta_{4,0} \setminus \{x_4, y_1\}$. All other deletions of $\Delta_{4,0}$ give ports isomorphic to $\Delta_{4,1}$, $\Delta_{4,2}$ or $\Delta_{4,3}$, or are not reduced. Note that $\Delta_{4,1} = \Delta_{4,0} \setminus z_1$, but checking that $\Delta_{4,0}$ is binary directly is more involved than constructing it from $\Delta_{4,1}$.

Theorem 10. *Let Δ be a reduced 4-homogeneous clutter without clones. Then, Δ is a binary matroid port if and only if Δ is isomorphic to either $\Delta_{4,0}$, or $\Delta_{4,1}$, or $\Delta_{4,2}$, or $\Delta_{4,3}$.*

The proof of Theorem 10 is long and entirely new, in the sense that it does not rely on previous results from either the matroid or the cryptographic communities. We give a very short sketch of the main ideas for the interested reader.

We start with a reduced and clone-free binary matroid port Δ; being reduced, the clutter Δ must contain at least three sets. We exploit the fact that the matroid $\mathcal{M}_\Delta$ is binary and the characterizations of Theorem 2 to find bounds on the sizes of the intersections of the sets in Δ. From this a careful case analysis follows, leading to the four clutters $\Delta_{4,0}, \Delta_{4,1}, \Delta_{4,2}$ and $\Delta_{4,3}$.

The final part of the proof consists in showing that the clutters $\Delta_{4,i}$, for $i \in \{0, 1, 2, 3\}$, are terminal, in the following sense: there is no reduced and clone-free binary matroid port that strictly contains $\Delta_{4,0}$; any reduced and clone-free binary matroid port that strictly contains $\Delta_{4,3}$ also contains a clutter isomorphic to $\Delta_{4,2}$; and any reduced and clone-free binary matroid port that strictly contains $\Delta_{4,1}$ or $\Delta_{4,2}$ is isomorphic to $\Delta_{4,0}$.

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